

REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

I. Introduction

Claims 36, 37, 39-41 and 44-47 are pending in this application. Claims 38, 42 and 43 have been cancelled. Claims 36 and 41 have been amended and new claims 46-47 have been added. Support for the amendment to claim 36 and for new claim 46 may be found on page 11, last paragraph (which incorporates by reference US application 10/613,071 which discloses an LED with regard to Figure 15), and support for the amendment to claim 41 and for new claim 47 may be found on page 4, last paragraph. No new matter was added.

II. The §112, ¶1 Rejection Should Be Withdrawn

Claims 38 and 43 are rejected under §112, ¶1 as lacking an adequate written description. Without acquiescing to the propriety of the rejection, claims 38 and 43 have been cancelled to expedite the prosecution of the present application and thus rendering the rejection moot.

III. The §112, ¶2 Rejection Should Be Withdrawn

Claims 36-45 are rejected under §112, ¶1 as being indefinite. The Office Action states that applicant has failed to give an adequate description of a “bulk semiconductor region”. Applicants respectfully disagree.

The term “bulk semiconductor material” has a well established meaning in the semiconductor art and means a three dimensional material. In other words, while a nanowhisker is defined as a quasi-one dimensional structure having at least two dimensions less than 1 micron (see paragraph bridging pages 1-2 of the specification), a bulk semiconductor material is a three dimensional structure having all three dimensions greater than 1 micron. For example, the on-line dictionary at www.infoplease.com/dictionary defines

“bulk” as having a magnitude in three dimensions (see exhibit attached hereto). Thus, a bulk semiconductor material is the opposite of a nanowhisker.

In response to the comments in the last paragraph on page 2 of the Office Action, applicants respectfully reply that the quasi-one dimensional sheath 8 around the nanowhisker 6 shown in Figure 2 is not an example of a bulk semiconductor region because the sheath 8 is not three dimensional. The polymer region 50 shown in Figure 5 is also not an example of a bulk semiconductor region because the polymer 50 in Figure 5 is not a semiconductor. However, semiconductor region 76 shown in Figure 7 is an example of a bulk semiconductor region because region 76 is three dimensional (i.e., it extends in three dimensions for more than a micron).

As discussed throughout the present specification, a bulk semiconductor material is a semiconductor material that is formed by methods other than VLS catalytic nanowhisker growth (see page 13, last paragraph, page 14, last paragraph, page 17, lines 24-26). Furthermore, a bulk semiconductor material has a different band gap and band bending compared to a nanowhisker (see page 18, lines 5-10 and page 19, lines 13-15). Thus, applicants respectfully submit that the term “bulk semiconductor region” is clearly defined and its scope is clear to one of ordinary skill in the art to satisfy §112, ¶2.

IV. The §102(b) Rejection Should Be Withdrawn

Claims 36-45 have been rejected under §102(b) as being anticipated by Yazawa. The Office Action asserts that the devices of Embodiment 1 and Figures 1, 2 and 8 of Yazawa anticipate the claims. This rejection is respectfully traversed.

Claim 36 has been amended to recite a light emitting diode. In contrast, Figures 1, 2 and 8 of Yazawa disclose a field effect transistor (FET). Thus, Yazawa does not anticipate claim 36 because the portion of Yazawa relied upon for the rejection does not teach every limitation of claim 36. One of ordinary skill in the art would also not be lead to modify the transistors of Figures 1, 2 and 8 of Yazawa to form a light emitting diode because a transistor has a different structure and function from a light emitting diode. For example, a field effect

transistor is generally a three terminal switching device while a light emitting diode is a two terminal light emitting device.

Claim 41 has been amended to recite that the nanowhisker is doped with a first conductivity type dopant. The method of making the transistor of Figures 1, 2 and 8 of Yazawa does not include intentionally doping the nanowhisker when a bulk semiconductor material surrounds the nanowhisker. Specifically, col. 6, lines 23-34 of Yazawa state:

The FET in FIG. 1 shows a case in which carriers are electrons. Electrons reach a drain electrode 3 from a source electrode 5 through a conductive semiconductor substrate (source) 11 and whisker channels 1. A material of a layer shown at 6 is selected in relationship with carrier generation in the channels. In case the whiskers themselves have conductivity, an insulating material is selected, and when the whiskers have no conductivity (undoped), a HEMT mechanism for instance, i.e., an n-type semiconductor having smaller electron affinity than that of the whiskers is selected. In this case, a band diagram at a junction portion between the whisker channels 1 and the n-type semiconductor layer 6 is as shown in FIG. 2, and a one dimensional electron gas (1 DEG) is confined in the whisker channels 1. [emphasis added]

In other words, Yazawa requires that the FET must have one of two structures: 1) doped nanowhisker 1 and insulating material 6 around the nanowhisker; or 2) undoped nanowhisker 1 and doped semiconductor material 6 around the nanowhisker. Yazawa does not teach a doped nanowhisker and forming a bulk semiconductor material 6 around the nanowhisker as recited in claim 41. In fact, a combination of a doped nanowhisker and a doped bulk semiconductor material 6 would probably render the device of Yazawa inoperative for the following reasons.

When the nanowhisker 1 of Yazawa is a doped semiconductor nanowhisker, it acts as a channel of the transistor. The insulating layer 6 is used to electrically isolate each nanowhisker 1 from the adjacent nanowhiskers (similar to a field oxide which is used to isolate adjacent active regions in a bulk transistor formed in a semiconductor substrate). If layer 6 was a doped semiconductor, then it would short each nanowhisker channel 1 to adjacent nanowhisker channels and would render the transistors inoperative.

When the nanowhisker 1 is an undoped semiconductor nanowhisker, a one dimensional electron gas (1 DEG) is confined by the n-doped layer 6 in the nanowhisker channels 1, as shown by the band diagram in Figure 2 of Yazawa. If the nanowhisker 1 was doped with the opposite conductivity type dopant (i.e., p-type dopant) from the n-type semiconductor layer 6, then this would disrupt the band structure shown in Figure 2 of Yazawa and may prevent or disrupt the one dimensional electron gas from forming in the nanowhisker. This would also render this transistor of Yazawa inoperative because the one dimensional electron gas is the conduction path between the source 3 and drain 5 electrodes of the transistor of Yazawa.

V. Conclusion

Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested. The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check or credit card payment form being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicants hereby petition for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date

8/21/07

By



FOLEY & LARDNER LLP

Customer Number: 22428

Telephone: (202) 945-6090

Facsimile: (202) 672-5399

Leon Radomsky

Attorney for Applicant

Registration No. 43,445